REMARKS

The Specification and claims have been reviewed for typographical and grammatical errors. A few minor errors were discovered, mostly of a typographical nature, such as a missing word. Various amendatory repairs have been requested. It is believed that none of these is controversial in the least, and that none introduces any new matter whatsoever. A reference to "42" in Figure 4 has been added on page 12, at an appropriate location where that circuitry is discussed. This, too, is believed to be free of new matter, as it is well supported by the Figures as originally filed.

The Examiner complained that reference character 37 was omitted from Figure 4 of the later filed Formal Drawings. A proposed new Figure 4 is supplied herewith that corrects this inadvertent omission. Antecedent basis is found in the informal drawing as originally filed. See the lower left corner of the informal figure 4: item 37 is the bottom input to the OR gate 38 that is just to the right of comparator 36.

As an aid in citing locations in a reference, let us adopt the following notational convention: lines 4 through 23 in col. 7 of Saito are referred to as Saito @ 7:4 - 23. When it is clear that Saito is the reference under consideration, we can simply say 7:4 - 23, and if only line 10 is needed, 2:10. Also, Saito @ 7:4 - 8:41 will be appreciated as indicating line 4 of col. 7 through line 41 of col. 8.

Turning now to the action on the merits, the allowance of Claim 1 is noted with appreciation.

Claim 2 was rejected under 35 USC 112 as not supported by the Specification: the detection transition circuit coupled to the delayed clock .... was said to be absent. This rejection is traversed. The TRANSITION DETECTOR (42) of Figure 4 as originally filed, and as described in the Specification at lines 5-23 of page 12, are antecedent support for the recited transition detection circuit of claim 2. The Examiner went on to complain that the incorporation of "System and Method for Adjusting a Sampling Time in a Logic Analyzer" on page 1 was inadequate support. That patent was incorporated as a safety measure, and while it is true that we have not (so far) introduced any of its text or drawings, we have provided Figure 4 and the above-noted text on page 12. That makes the need for any critical reliance on "System and Method for Adjusting a Sampling Time in a Logic Analyzer" most unlikely, and applicant declines at present to transplant material from "System and Method for Adjusting a Sampling Time in a

Logic Analyzer" into the present case. It seems most probable that the Examiner simply overlooked the stuff on page 12 and the TRANSITION DETECTOR of Figure 4.

Claim 2 was further rejected under §112 as indefinite for reciting the "transition detector coupled to the delayed clock signal and to the delayed logical data ..." With all due respect, this rejection is not understood, unless it is a mere formal consequence of the other §112 rejection, possibly abetted by a confusion relating to the incorporated patent. In any event, it does not appear to applicant that there is any §112 defect in the claim as it stands, and the structural arrangement of its elements and the manner of their individual and collective operation is covered in considerable detail in Specification's description of Figure 4, which runs from line 18 on page 9 to the end of page 13. This rejection is respectfully traversed.

Claim 2 was also rejected under 35 USC 103 over Saito (US 56,210,712) in view of Haag (US 4,445,192). This rejection is also respectfully traversed. Saito does not disclose the claimed transition detector operating in conjunction with the claimed threshold detector. The claimed structure produces an output that indicates that the data signal was at about the threshold voltage at about the expiration of a delay in the clock signal. (That is the meaning of the transition detector circuit outputs that get counted.) Saito has some sort of servo that varies a threshold voltage to drive a level shifter for optimum operation (most of his figures), and he has a variable delay that is servoed against errors found by comparing data against a reference pattern (see 9:10 - 31). He simply does not discover the voltage of a data signal at a variable point in time by noticing a transition in that data signal about a threshold during a selected length of time anchored by the variable point in time, which is what the claimed structure does. Saito does not suggest any such manner of operation.

Nor does Saito combined with Haag show or suggest the recited combination of Claim 2. Haag is a logic analyzer that simply produces a data structure that shows what the logical values of a collection of signals were at clock cycles of interest. There is no attempt to describe voltage variation within a clock cycle as a function of time.

Thus, on the basis of the arguments set out above, claims 1 and 2 are believed to comply with 35 USC 112 and 35 USC 103, and the Examiner is respectfully, but earnestly, urged to withdraw the rejections.

THEREFORE, re-examination is requested, and favorable action is respectfully solicited.

Respectfully submitted,

Richard A. Nygaard, Jr.

By Edward L Miller

Edward L. Miller
Agent of Record
Reg.# 29,331

24 October 2003
(970) 679-3677
Agilent Technologies, Inc.
815 14th St. S.W.
Loveland, Colorado 80537
ELM:elm